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PTO/SB/08A (08-00)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known

Application Number 10/743894
Filing Date 12/17/2003
First Named Inventor Madurawe, Raminda U.
Group Art Unit 2819
Examiner Name D. de
Attorney Docket Number

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
/		4,708,218		Carter	11-10-1987	
		4,870,302		Freeman	09-28-1989	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	r*
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if Known <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td>10/79,3894</td> </tr> <tr> <td>Filing Date</td> <td>12/17/2003</td> </tr> <tr> <td>First Named Inventor</td> <td>Madurawe, Raminda U.</td> </tr> <tr> <td>Group Art Unit</td> <td>2819</td> </tr> <tr> <td>Examiner Name</td> <td>D. Le</td> </tr> <tr> <td>Attorney Docket Number</td> <td></td> </tr> </table>		Application Number	10/79,3894	Filing Date	12/17/2003	First Named Inventor	Madurawe, Raminda U.	Group Art Unit	2819	Examiner Name	D. Le	Attorney Docket Number	
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Examiner Name	D. Le														
Attorney Docket Number															
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
he		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA	<input checked="" type="checkbox"/>
h		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 89-171, McGraw-Hill, USA	<input type="checkbox"/>
he		E. AHMED, J. ROSE, "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA, 2000.	<input type="checkbox"/>
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Examiner Signature	D. Le	Date Consid red	8/5/05
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